

FIG 1

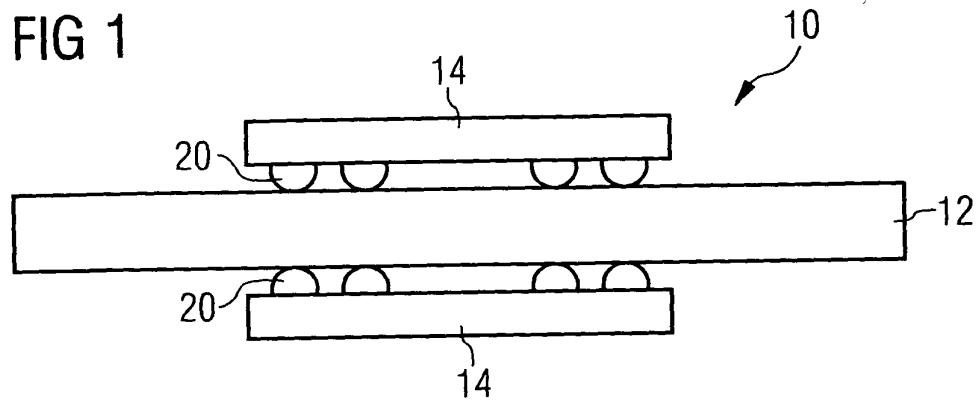


FIG 2A

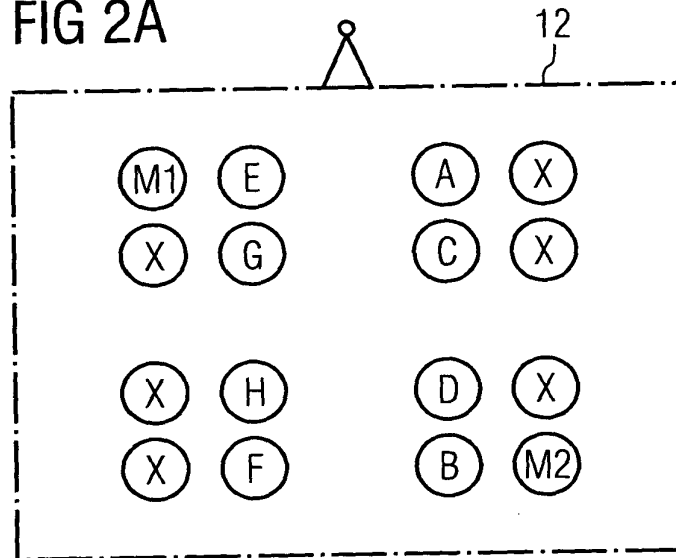


FIG 2B

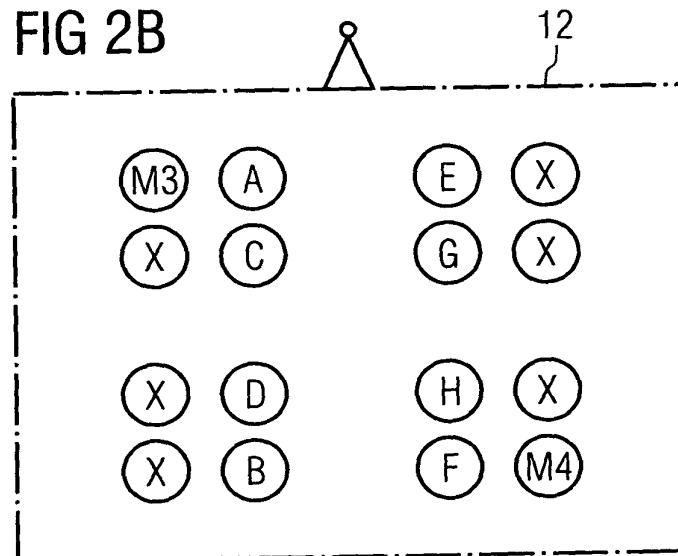


FIG 3

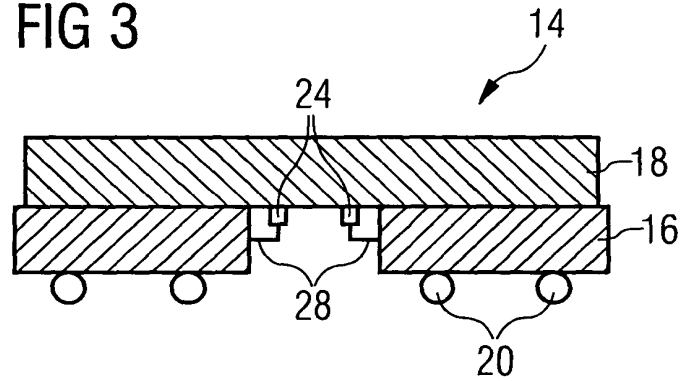


FIG 4

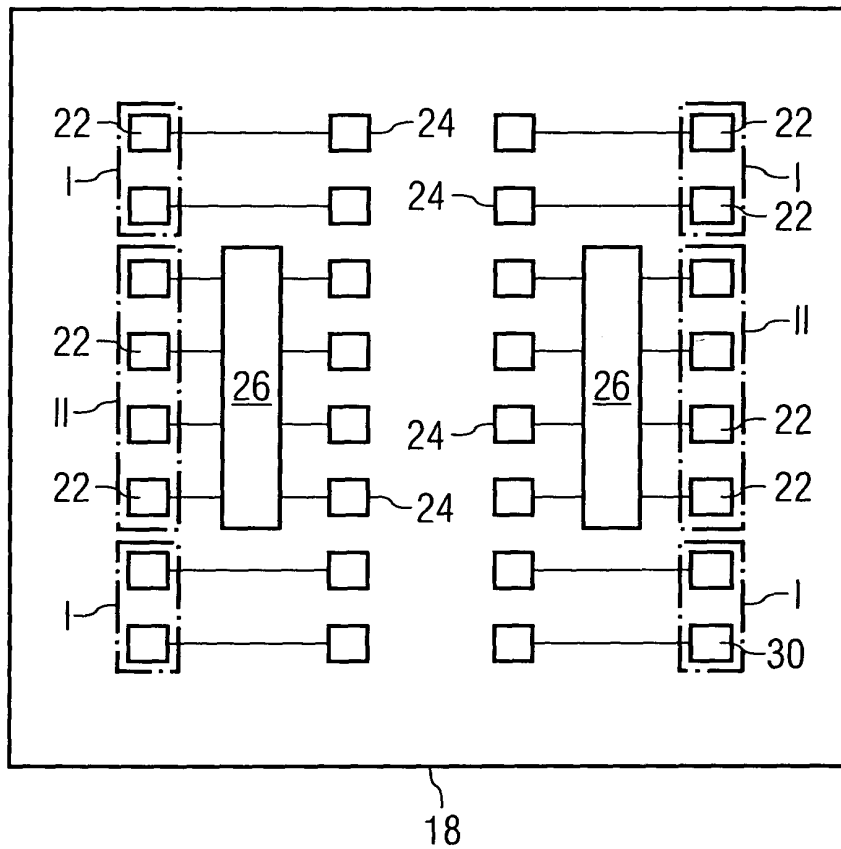


FIG 5A

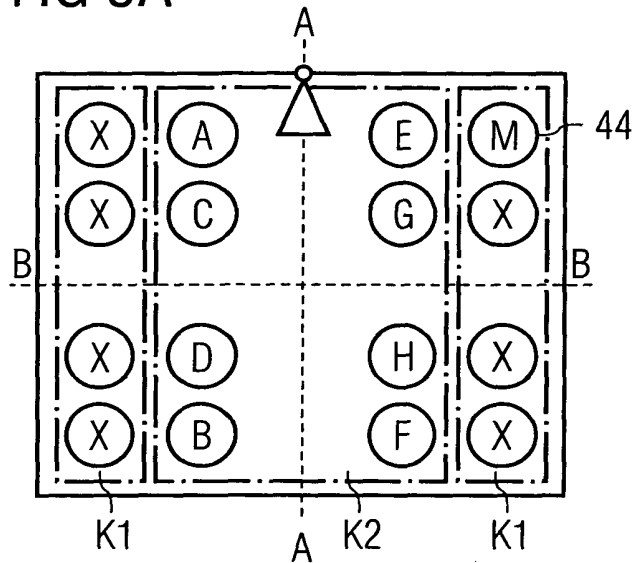


FIG 5B

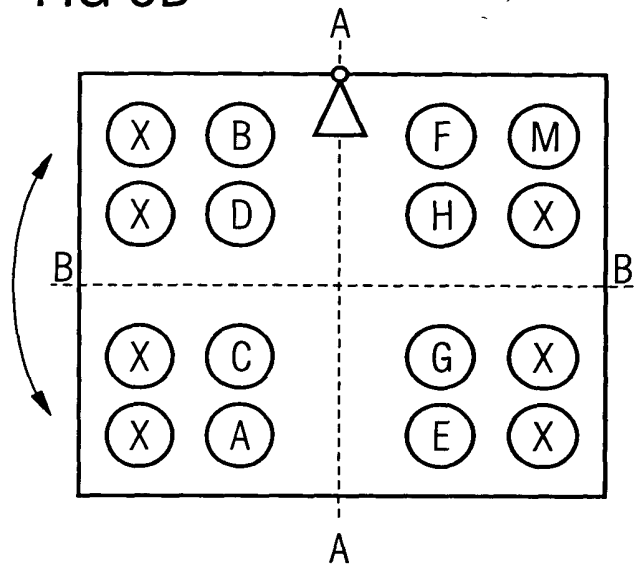


FIG 5C

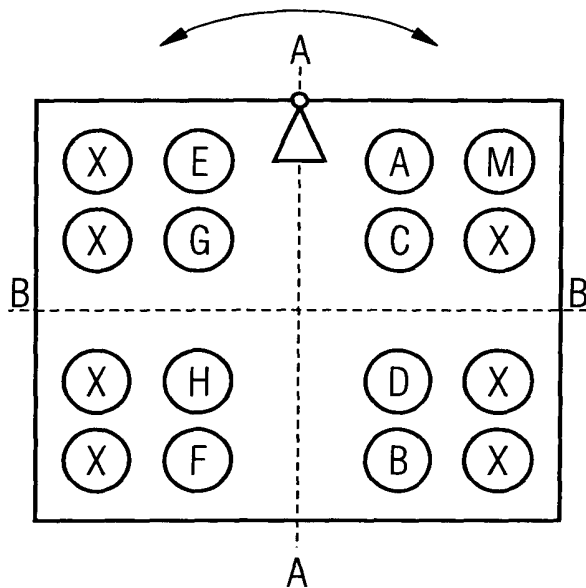


FIG 5D

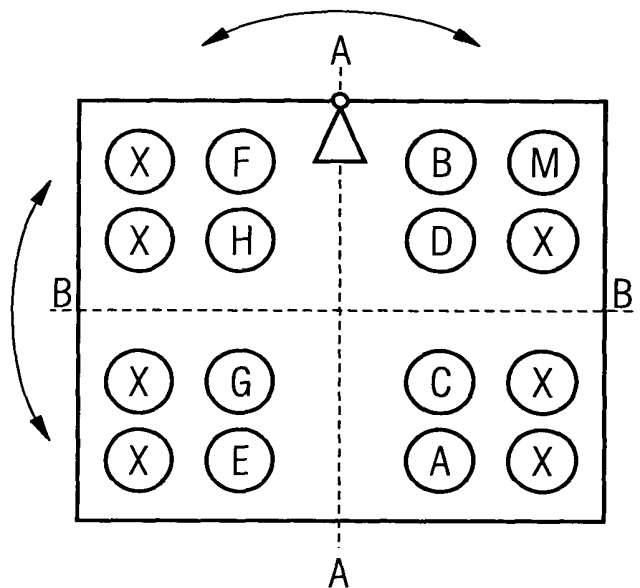


FIG 6

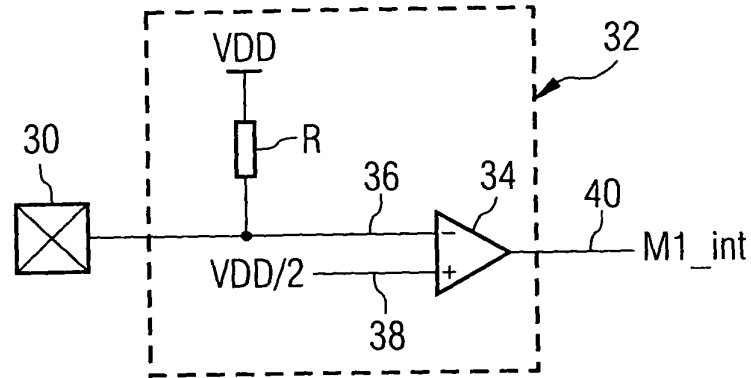


FIG 7A

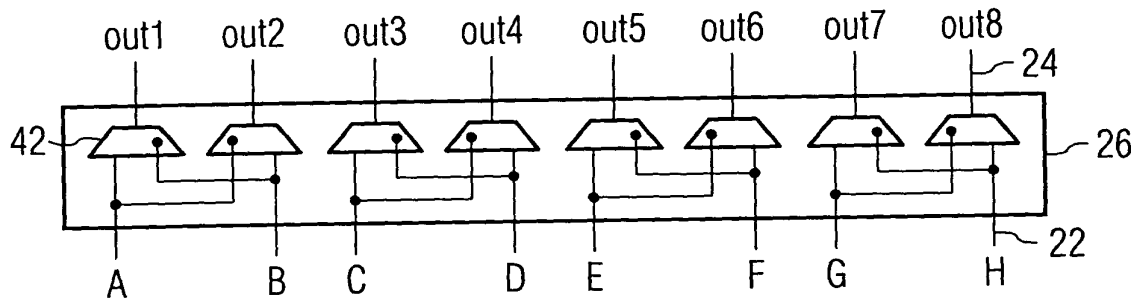
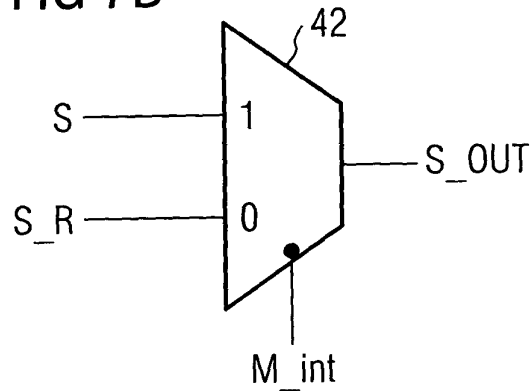


FIG 7B



M_int	S_OUT
1	S
0	S_R

FIG 8

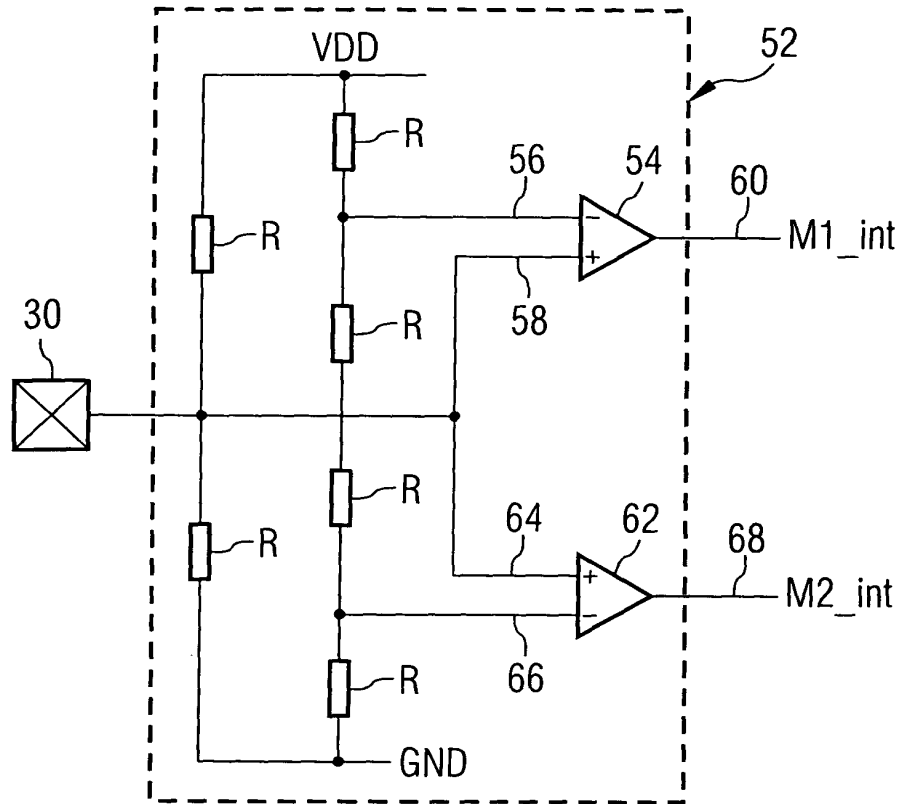
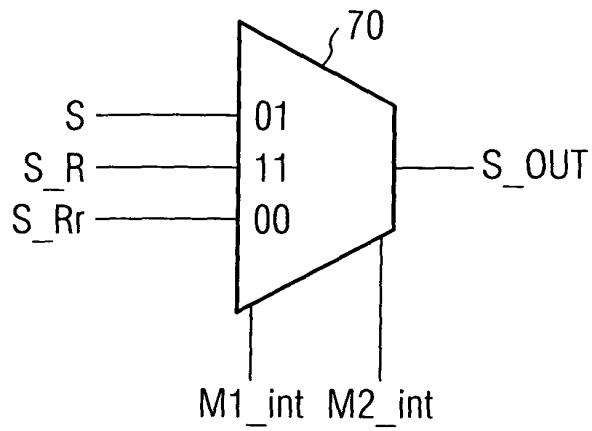


FIG 9



M1_int	M2_int	S_OUT
0	1	S
1	1	S_R
0	0	S_Rr

FIG 10

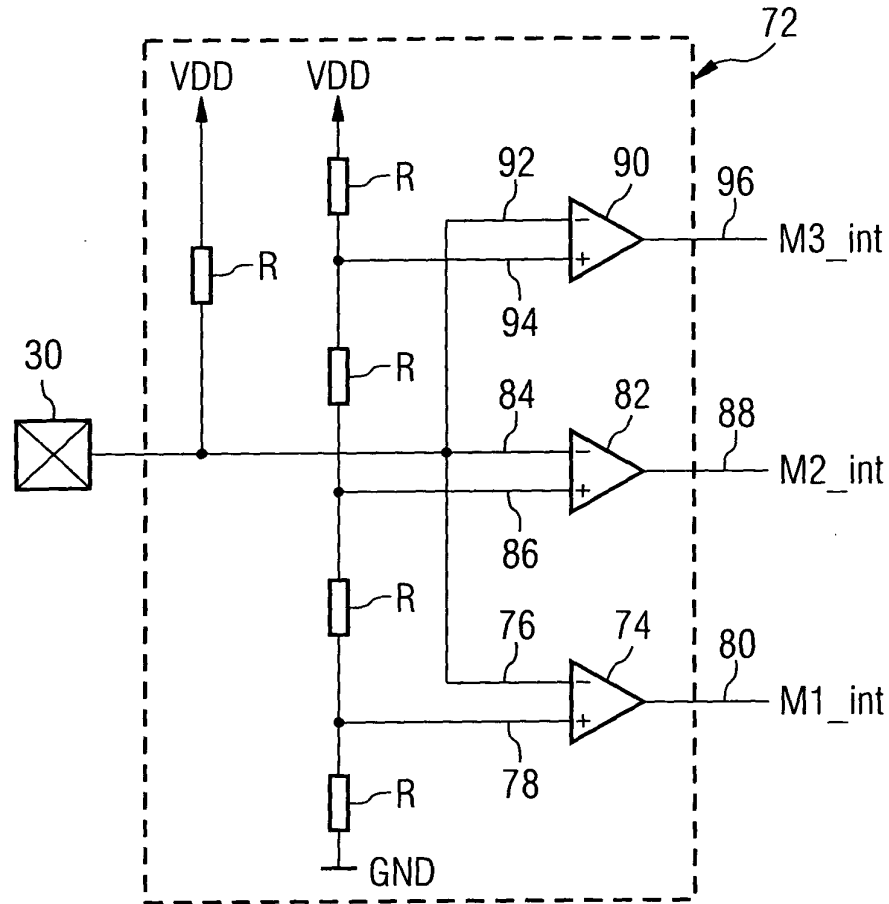
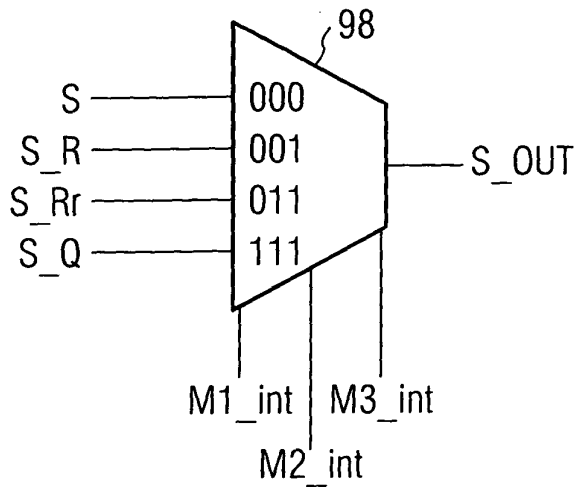


FIG 11



M1_int	M2_int	M3_int	S_OUT
0	0	0	S
0	0	1	S_R
0	1	1	S_Rr
1	1	1	S_Q